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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,596	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,9,11,12 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,9,11,12 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 1/4/2005.

Claim Rejections - 35 USC § 112

2. Claims 1, 3-4, 9 and 11-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 1 and 9, the limitation "an off-chip memory module" neither clearly disclosed in the drawing nor described in the specification. Although Applicant pointed out such limitation is illustrated with reference to figures 1 and 2 of Applicant's specification, it is noted that figures 1 and 2 of Applicant's specification merely discloses the system memory (210, figure 1) having memory modules (220, 230, 240 and 250, figure 2), which does not specify the memory module as an off-chip memory module or on-chip memory module. In addition, the specification fails to disclose a detailed structure of the motherboard such that the off-chip system memory can be an external module from a computer system or a system memory external from a memory controller or else. Note the specification does not clearly define the claimed limitations. Thus, the off-chip memory module as defined in the claims 1 and 9 was not described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 3-4 and 11-12 are also rejected because of depending on claims 1 and 9, respectively, containing the same deficiency.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 20, Saulsbury teaches a memory module (103, figure 1) including at least one memory device (104, figure 1) and a data cache (122, figure 1), coupled to an eviction buffer (106, figure 1), each coupled to the memory device (col. 3 lines 52-62), the data cache controlled by a plurality of commands delivered by a memory controller (102, figure 1) over a bus, the memory module to receive a write back command to cause a previous line of data evicted from the data cache and store within the eviction buffer to be written out of the eviction buffer to the memory device (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Regarding claim 21, Saulsbury teaches to the data cache to evict the previous line of data from the data cache into the eviction buffer according to an eviction signal received from the memory controller (col. 11 lines 40-47).

Regarding claim 22, Saulsbury discloses the write-back command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-4, 9, 11-12, 16-19 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 1, Stracovsky discloses a memory controller (104, figure 1B) comprising an array of tag address storage locations (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage locations, the command sequencer and serializer unit to control an off-chip system memory (108, figure 1B), the memory controller coupled to the off-chip system memory via a memory bus (220, figure 1B), the command sequencer and serializer unit to cause a current line of data to be written from

the command sequencer and serializer unit to a memory module within the off-chip system memory (col. 6 line 21 through col. 8 line 32, col. 11 line 22 through col. 12 line 19 and col. 13 lines 8-47) Stracovsky differs from the claimed invention in not specifically teaching a data cache and an eviction buffer located on at least one memory module of a system memory and the command sequencer and serializer unit to cause the current line of data to be written from the command sequencer and serializer unit to the data cache and to cause a previous line of data to be evicted out of data cache to the eviction buffer location on the memory module. However, Saulsbury teaches the computer system (100, figure 1) comprising a memory controller (102, figure 1) and a system memory (103, figure 1) including a data cache (122, figure 1) and an eviction buffer (106, figure 1) located on a memory module of the system memory so that a memory accessing operation comprises a command to cause a current line of data to be written to the data cache (col. 7 lines 42-48) and to cause a previous line of data, i.e., victim cache line, to be evicted out of the data cache to the eviction buffer in order to reduce cache miss rate (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having the data cache and the eviction buffer located on at least one memory module of the system memory and the command sequencer and serializer unit to cause the current line of data to be written from the command sequencer and serializer unit to the data cache and to cause a previous line of data to be evicted out of data cache to the eviction buffer location on the memory module, as per teaching of Saulsbury, because it reduces cache miss rate.

Regarding claim 3, Saulsbury discloses the command sequencer and serializer to deliver a write-back command to the data cache associated with the memory module, the write back

command to cause the previous line of data stored in the eviction buffer to be written out to a second memory module memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines .37-64).

Regarding claim 4, Saulsbury discloses the write-back command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 9, Stracovsky discloses a system comprising a processor (102, figure 1B), a memory controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B), the memory controller including an array of tag address storage location (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage location (col. 7 line 24 through col. 8 line 2 and col. 10 line 46 through col. 11 line 15), and an off-chip system coupled to the memory controller via a memory bus (220, figure 1B), the off-chip system memory including at least two memory (device type 1 - device type N, figure 1C). Stracovsky differs from the claimed invention in not specifically teaches each memory module including at least one memory device and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer. However, Saulsbury teaches such (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Stracovsky in having each memory module including at least one memory device and a data cache coupled to

the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer, as per teaching by Saulsbury, because it reduces the cache miss rate over conventional data caches that store data cache lines that are less than full-width.

Regarding claim 11, Saulsbury discloses the memory controller to deliver a write-back command to the data cache, the write-back command to cause the previous line to written out of the eviction buffer to the memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 12, Saulsbury discloses the write-back command including way information and back address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 16, Stracovsky discloses a memory controller (104, figure 1B) comprising an array of tag address storage locations (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage locations, the command sequencer and serializer unit to control an off-chip system memory (108, figure 1B) (col. 6 line 21 through col. 8 line 32, col. 11 line 22 through col. 12 line 19 and col. 13 lines 8-47) Stracovsky differs from the claimed invention in not specifically teaching a data cache and an eviction buffer located on at least one memory module of a system memory and the command sequencer and serializer unit to deliver a write back command to the eviction buffer associated with the memory module, wherein the write back command causes a previous line of data evicted from the data cache and stored in the eviction buffers, to be written out tot a memory

device of the memory module. However, Saulsbury teaches the computer system (100, figure 1) comprising a memory controller (102, figure 1) and a system memory (103, figure 1) including a data cache (122, figure 1) and an eviction buffer (106, figure 1) located on a memory module of the system memory so that a memory accessing operation comprises a write back command to cause a previous line of data, i.e., victim cache line, to be evicted out of the data cache and stored in the eviction buffer to be written out to a memory device of the memory module in order to reduce cache miss rate (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having data cache and eviction buffer located on at least one memory module of a system memory and the command sequencer and serializer unit to deliver a write back command to the eviction buffer associated with the memory module, wherein the write back command causes a previous line of data evicted from the data cache and stored in the eviction buffers, to be written out tot a memory device of the memory module, as per teaching of Saulsbury, it reduces the cache miss rate.

Regarding claim 17, Saulsbury teaches to issue an eviction signal to the data cache to evict the previous line of data from the data cache into the eviction buffer (col. 11 lines 40-47).

Regarding claim 18, Saulsbury teaches to issue the write back command to cause the previous line of data to be written out of the eviction buffer to the memory device once the memory device is idle (col. 13 lines 12-52).

Regarding claim 19, Saulsbury teaches a memory accessing operation comprising a command to cause a current line of data to be written to the data cache (col. 7 lines 42-48) and to

cause a previous line of data, i.e., victim cache line, to be evicted out of the data cache to the eviction buffer (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Regarding claim 23, Stracovsky discloses a system memory comprising at least two memory modules (figures 1A and 1C). Stracovsky differs from the claimed invention in not specifically teaching each memory module including at least one memory device and a data cache coupled to an eviction buffer, each coupled to the memory device. However, Saulsbury teaches a memory module (103, figure 1) including at least one memory device (104, figure 1) and a data cache (122, figure 1), coupled to an eviction buffer (106, figure 1), each coupled to the memory device (col. 3 lines 52-62). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having each memory module including at least one memory device and a data cache coupled to an eviction buffer, each coupled to the memory device, as per teaching of Saulbury, in order to reduce cache miss rate.

Regarding claim 24, Saulsbury discloses a memory module to receive a write back command to cause a previous line of data evicted from the data cache to be written out of the eviction buffer to the memory device (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Regarding claim 25, Saulsbury teaches to cause store a current line of data within a data cache (col. 7 lines 42-48) and to cause a previous line of data from the data cache to be evicted out of the data cache to the eviction buffer located on the memory module in response to a command (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Response to Arguments

7. Applicant's arguments filed 1/4/2005 have been fully considered but they are not persuasive.

In response to applicant's argument that "the off-chip system memory" is illustrated with reference to figures 1 and 2 of the specification, it is noted that figures 1 and 2 of Applicant's specification merely discloses the system memory (210, figure 1) having memory modules (220, 230, 240 and 250, figure 2), which does not specify the memory module as an off-chip memory module or on-chip memory module. Thus, the rejection under 35 U.S.C. § 112 is maintained.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that Saulsbury is directed to an integrated processor memory device comprising a main memory a CPU, a victim cache and a primary cache, which is different from Stracovsky, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation of combining Saulsbury with Stracovsky is to reduce the cache miss rate over conventional data caches that store data cache lines that are less than full-width, as cited in Sualsbury (col. 15 lines 25-45).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., off-chip system memory) are not recited in the rejected claims 20-25. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that Saulsbury fail to show a write back command to cause the previous line of data to be written out of the eviction buffer to the memory device, it is noted that Saulsbury clearly teaches to write out the previous line of data, i.e., dirty victim primary data cache line, of the eviction buffer to the memory device (col. 13 lines 23-66). Thus, Saulsbury is enough to reject the broad claimed limitations.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Marshall, Jr. et al. (US PAT. 6,134,634) discloses a method for preemptive cache write-back (abstract). Arimilli et al. (US PAT. 6,128,707) discloses a method for selectively adapting the burst mode write-back from cache to main memory consistent with the extent of a cache line actually modified by a processor (col. 1 line 61 through col. 2 line 36). Lentz et al. (US PAT. 5,499,384) discloses an I/O controller serving as a queuing structure to maximize the memory bandwidth of the memory bus and increase the data flow throughput (abstract). Foley (US PAT. 5,537,575) discloses a system for handling cache memory victim data for updating main memory (abstract).

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:30 AM-6:00 PM, and alternate Monday 8:30 AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li
Patent Examiner
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MATTHEW D. ANDERSON
PRIMARY EXAMINER